Address Setting

As an aid to setting the base address DIP switch, run the INSTALL.EXE program from the DOS prompt. INSTALL.EXE, a graphical switch position display program, will round your address to the nearest 4 bit boundary and display the correct positions of the switches on the base address DIP switch. Set the ML8-P base address switches to correspond with the displayed settings. Alternatively, you can look up the correct switch settings in the ADDRESS SETTINGS table on the following page.

ML8-P uses 4 consecutive I/O addresses that are set by the BASE ADDRESS DIP switch to be on a 4-bit boundary anywhere in the PC decoded I/O space. The ML8-P's address may be changed to avoid conflict with other peripheral cards or previously reserved internal I/O addresses. The PC AT's I/O address space extends from 256-1018 (Hex 100-3FA) allowing for the use of more than one ML8-P in a single computer. Most of this space is available if your system does not have one or more of the components listed in the table below. H300 is a normally free area and is the recommended address for installing the board. The reserved I/O addresses for standard devices are as follows:

ADDRESS(Hex)	DEVICE
000-1FF	Internal system
200-20F	Game
210-217	Expansion unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	LPT2:
2F8-2FF	COM2:
300-31F	Prototype card
320-32F	Hard disk
3F8-3FF	COM1:

ADDRESS(Hex)	DEVICE
378-37F	LPT1:
380-38C	SDLC comm.
380-389	Binary comm. 2
3A0-3A9	Binary comm. 1
3B0-3BF	Mono dsp/LPT1:
3C0-3CF	Reserved
3D0-3DF	Color graphics
3E0-3E7	Reserved
3F0-3F7	Floppy disk

This covers the standard I/O options but if you have special peripherals installed, they may use I/O addresses not listed in the table above. Memory addressing is separate from I/O addressing so there is no possible conflict with any add-on memory that may be in your computer. A good choice is to put the ML8-P at base address Hex H300 or H310 (decimal 768 or 784).

The only other setting on the ML8-P is the choice of hardware interrupt level. If you are not going to use interrupts in your programming, the interrupt jumper can be left in the "X" (inactive) position. If you intend to use interrupts, set the jumper to a level that is not in use by any other peripheral board.

Programming the ML8-P Board

The ML8-P is programmed using input/output instructions. In BASIC, these are the INP (X) and OUT X,Y functions. Most high level languages have equivalent instructions. Use of these functions involves setting registers and providing I/O addresses.

I/O Address Map of ML8-P

The following is the I/O address map of the ML8-P.

ADDRESS	READ	WRITE
Base Address + 0	Always zero	Start A/D conversion
Base Address + 1	A/D valid data (8 bit)	Start A/D conversion
Base Address + 2	Status register	Control register

The ML8-P has an I/O address map that is a subset of the AIO8-P (8-bit mode), it uses only the first 4 addresses but the register format and functions are identical. This maintains hardware compatibility with Industrial Computer Source's model AIO8-P A/D board. So, the ML8-P can be used with existing software that have drivers for the AIO8-P (Labtech Notebook, for example).

Starting the A/D Converter

Start the A/D conversion by writing to BASE ADDRESS + 0 or BASE ADDRESS + 1. The data written to start the conversion is irrelevant. The A/D conversion takes about 30 microseconds to complete. Its progress is monitored at bit 7 of the status register.

The ML8-P uses the AD7574 8-bit A/D converter. One of the features of this converter is that data from the previous conversion must be read before another conversion is allowed.

Reading the A/D Data

After the conversion, the data is read from BASE ADDRESS + 1. The data format is:

BIT POSITION	D7	D6	D5	D4	D3	D2	D1	D0
BASE ADDRESS + 1	B7	B6	B5	B4	B3	B2	B1	B0
	MSB							LSB

BASE ADDRESS + 0 always returns zero when read, this maintains compatibility with the 12-bit A/D data of the AIO8-P.

The A/D data bits B7-B0 correspond to an offset binary code:

BINARY	HEX	DECIMAL	ANALOG INPUT VOLTAGE
0000 0000	00	0	-5.000 V (- Full scale)
0000 0001	01	1	-4.961 V
-	-	-	-
0100 0000	40	64	-2.500 V (- 1/2 scale)
-	-	-	-
1000 0000	80	128	0 V (zero)
1000 0001	81	129	+0.039 V
-	-	-	-
1100 0000	C0	192	+2.500 V (+1/2 scale)
-	-	-	-
1111 1111	FF	255	+4.961 (+Full scale)

The ML8-P Control Register

The control register sets the multiplexer (channel) address, enables and disables interrupts, and provides output data to the four general purpose digital outputs OP1-OP4. The control register is a write only register located at I/O address BASE ADDRESS + 2 (the same location as the status register). The data format of the control register is as follows.

BIT POSITION	D7	D6	D5	D4	D3	D2	D1	D0
BASE ADDRESS + 2	OP4	OP3	OP2	OP1	INTE	MA2	MA1	MA0
	MSB							LSB

The bits have the following significance:

OP4-OP1: These bits correspond to the four general purpose digital output lines OP1 through OP4. Use these lines for external control functions, for example, driving an input sub-multiplexer to increase the number of analog input channels. A 16-channel multiplexer on each of ML8-P's 8 analog channels expands the system to 128 channels.

INTE: ML8-P generated interrupts are enabled onto any of the selected PC interrupt levels 2-7 if INTE = 1 (logic high). Interrupts are disabled if INTE = 0 (logic low). Interrupts from the INT.IN input (pin 24) are passed through to the selected level and are rising edge triggered. It is the programmer's responsibility to set up an interrupt handling routine, interrupt vectors and initialize the 8259 interrupt controller on the PC processor board. Writing to the control register will clear the IRQ bit of the status register.

MA2-MA0: These bits select the current analog multiplexer channel address as follows:

MA2	MA1	MA0	CHANNEL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The multiplexer channel address is determined by reading the status register.

During power up, when the RESET line is asserted, the ML8-P control register is cleared. This ensures that ML8-P interrupts are disabled, sets digital outputs OP1-4 to zero and sets the multiplexer channel address to zero.

The ML8-P Status Register

The status register provides information on the operation of ML8-P. It is a read only register at I/O BASE ADDRESS + 2 and has the following format:

BIT POSITION	D7	D6	D5	D4	D3	D2	D1	D0
BASE ADDRESS + 2	EOC	IP3	IP2	IP1	IRQ	MA2	MA1	MA0
	MSB							LSB

The bits have the following significance:

EOC: End of Conversion. If EOC is high (Logic 1) the A/D is busy performing a conversion. Data should not be read in this condition as it will be invalid. Wait for the EOC to return to logic 0 signifying valid data available.

IP3 - IP1: These bits correspond to the three digital input port lines IP3, IP2 and IP1. They may be used for any digital input data.

IRQ: After generating an interrupt to the processor, IRQ is set to logic high (1). It is reset to logic low (0) by a write to the control register. This provides a means of acknowledging or "handshaking" ML8-P interrupts. Interrupts are latched in an internal flip-flop on the ML8-P board. The state of this flip-flop corresponds to the INT bit in the STATUS register. The interrupt flip-flop is cleared by a write to the CONTROL register. Service routines should acknowledge and re-enable the interrupt flop.